WHAT IS CLAIMED IS:

1. A memory controller comprising:

a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;

a storage unit coupled to said control unit;

an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;

wherein said control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and

wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from said memory subsystem and to write a corrected version of said data within said memory subsystem.

2. The memory controller as recited in claim 1, wherein said error detection and correction unit is further configured to provide said corrected version of said data in response to said subsequent read of said data.

3. The memory controller as recited in claim 1, wherein said indication includes an address in said memory subsystem of said erroneous data corresponding to said read request.

4. The memory controller as recited in claim 1, wherein said control unit is further configured to inhibit accepting an additional memory read request in response to said indication.

5. The memory controller as recited in claim 4, wherein said control unit is further configured to accept said additional memory read request in response to said subsequent read of said data from said memory subsystem and a corrected version of said data being written to said memory subsystem.

6. A data processing system comprising:

a processor;

a memory subsystem configured to store data;

a system controller including a memory controller coupled between said processor and said memory subsystem, wherein said memory controller includes:

a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;

a storage unit coupled to said control unit;

an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;

wherein said control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and

wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from said memory subsystem and to write a corrected version of said data within said memory subsystem.

7. The data processing system as recited in claim 6, wherein said error detection and correction unit is further configured to provide said corrected version of said data in response to said subsequent read of said data.

8. The data processing system as recited in claim 6, wherein said indication includes an address in said memory subsystem of said erroneous data corresponding to said read request.

9. The data processing system as recited in claim 6, wherein said control unit is further configured to inhibit accepting an additional memory read request in response to said indication.

10. The data processing system as recited in claim 9, wherein said control unit is further configured to accept said additional memory read request in response to said subsequent read of said data from said memory subsystem and a corrected version of said data being written to said memory subsystem.

11. A method of correcting erroneous data in a memory of a memory subsystem, said method comprising:

reading data including an associated error correction code from said memory subsystem in response to a memory read request;

receiving said data and determining whether an error exists in said data based upon said associated error correction code;

storing an indication that said data corresponding to said memory read request is erroneous; and

subsequently detecting said indication and responsively performing a subsequent read of said data from said memory subsystem and writing a corrected version of said data within said memory subsystem.

12. The method as recited in claim 11 further comprising providing said corrected version of said data in response to said subsequent read of said data.

13. The method as recited in claim 11, wherein said indication includes an address in said memory subsystem of said erroneous data corresponding to said read request.

14. The method as recited in claim 11 further comprising inhibiting accepting an additional memory read request in response to said indication.

15. The method as recited in claim 14 further comprising accepting said additional memory read request in response to performing said subsequent read of said data from

said memory subsystem and to said writing of said corrected version of said data to said memory subsystem.

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